

an addressing circuit which enables the combined photodiode outputs stored on said pixel's intrinsic capacitance to be read out in response to an address input.

9. (twice amended) A photodetector array with selectable resolution, comprising:

a plurality of photodetectors;

a switching circuit which configures neighboring ones of said photodetectors into active pixels by directly summing at each pixel the outputs of multiple photodetectors into an aggregated pixel output, said photodetector outputs summed at each pixel arranged such that their outputs are switchably connected to a common pixel node, said aggregated pixel output stored on said pixel's intrinsic capacitance prior to being read out;

wherein said switching circuit is electronically switchable to aggregate said photodetector signals according to at least two different selectable pixellization schemes with differing resolutions, such that said switching circuit combines photodetector signals according to at least two different, electronically selectable configurations: a first configuration in which each pixel output is a sum of two neighboring photodiodes; and a second configuration in which each pixel output is a sum of at least three photodiodes; and

a plurality of addressable interface circuits, each of which enables the aggregated pixel output stored on a respective one of said pixel's to be read out in response to an address input.

15. (twice amended) A photodetector array, comprising a plurality of active pixels, said array of pixels comprising a plurality of pixels arranged into at least three horizontal rows and vertical columns,

wherein each pixel comprises an association of at least two

subpixels arranged such that their outputs may be switchably connected to a common pixel node;

and wherein the outputs of said subpixels are switchably combined into at least two different grouping arrangements, to give at least two different selectable pixel configurations, wherein said at least two different grouping arrangements comprises two different grouping arrangements, one of which combines the outputs of two adjacent subpixels in a given vertical column, and the other of which combines the outputs of three adjacent subpixels in said given vertical column,

each of said pixels having an intrinsic capacitance which stores said combined subpixel outputs prior to their being read out, and

an addressing circuit which enables the combined subpixel outputs stored on said pixel's intrinsic capacitance to be read out in response to an address input.

REMARKS

This amendment is in response to the Office Action dated 9/19/02. Entry of this Amendment and reconsideration of this application are respectfully requested.

Claim Rejections under §103

Claims 1, 5, 9 and 13-15 were rejected as obvious over a patent to Arques et al. in view of a patent to Wilder et al.

In response, claims 1, 9 and 15 have been amended, as discussed below:

Claim 1

Claim 1 is directed to a photodetector array comprising a plurality of addressable active pixels. Each pixel in the array